REMARKS

Favorable reconsideration of this application is respectfully requested in view of the amendments above and the following remarks. By virtue of the foregoing amendments, Claims 1-12 have been amended. Thus, Claims 1-13 remain pending in the present application.

No new matter has been presented by way of the claim amendments and such amendments are deemed unobjectionable. Entry thereof is respectfully requested.

Attached hereto is a marked up version of the changes made to the claims by the present amendment. The attached page is captioned "Version With Markings to Show Changes Made."

Amendment to the Specification

The present specification has been amended in minor respects to correct a reference numeral error. More specifically, on page 8, line 22, reference numeral 330 has been amended to read 335 to be consistent with other references to numeral 335 in the specification and the drawings.

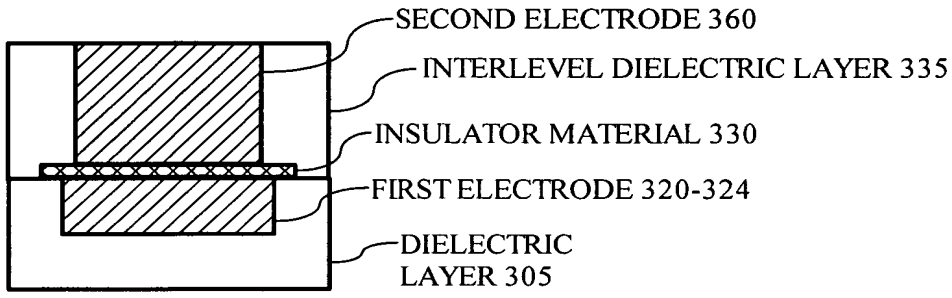
No new matter has been introduced by way of this amendment to the specification.

Claim Rejection Under 35 U.S.C. §102

Claims 1-4 and 7-13 have been rejected under 35 U.S.C. §102(e) as allegedly being unpatentable over the disclosure contained in U.S. Patent No. 6,162,680 to Lou. This rejection is respectfully traversed because Claims 1-4 and 7-13 are patentably distinguishable over the disclosures contained in this document.

Claim 1 relates to a method of forming a by-pass capacitor on a multi-level metallization device. In the method, a first electrode is formed in a first dielectric layer of the multi-level metallization device. A substantially thin insulator layer is deposited over the first dielectric layer of the multi-level metallization device. In addition, a second electrode is formed in a second dielectric layer over the substantially thin insulator layer.

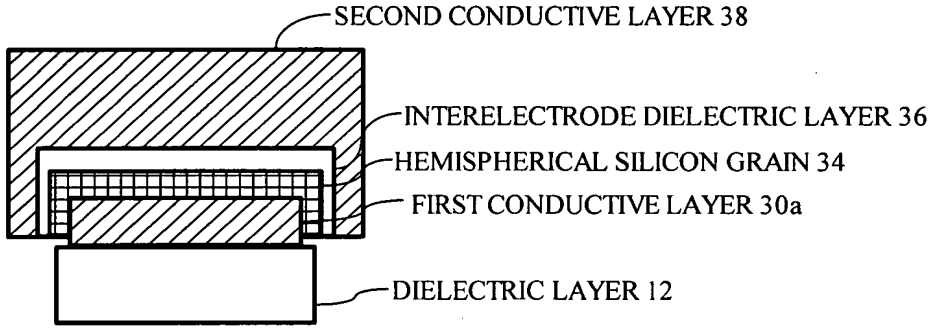
The following diagram may represent the by-pass capacitor formed through implementation of the method set forth in Claim 1. It is to be understood, that the following figure is merely a representation of a possible capacitor configuration based upon the steps set forth in Claim 1. Therefore, the figure below is not intended to limit the invention in any respect but is provided to assist in illustrating the differences between the present invention and the disclosure contained in Lou.



As can be seen in the above figure, the first electrode 320-324 is formed in the dielectric layer 305 and the second electrode 360 is formed in the interlevel dielectric layer 335. An insulator material 330 is positioned between the first electrode 320-324 and the second electrode 360.

In contrast, Lou discloses a method for forming a DRAM capacitor which differs from the elements set forth in Claim 1 of the present invention. As seen in figure six, Lou discloses that the capacitor formed through compliance with the disclosed method steps results in a capacitor having a much different configuration than the one illustrated above.

The following figure may represent the capacitor formed through implementation of the method disclosed by Lou:



As this figure illustrates, the first conductive layer 30a is not formed in the dielectric layer 12. In addition, the second conductive layer 38 is not formed in the interelectrode dielectric layer 36. Instead, the interelectrode dielectric layer 36 is formed in the second conductive layer 38. In addition, a hemispherical silicon grain 34 is placed between the first conductive layer 30a and the interelectrode dielectric layer 36.

At least by virtue of the above-described differences in the methods set forth in Claim 1 of the present invention and the disclosure contained in the Lou document, it is respectfully submitted that Lou cannot anticipate Claim 1. Accordingly, the invention set forth in Claim 1 of the present invention is patently distinguishable over the disclosure contained in Lou.

Claims 2-13 are also allowable by virtue of their dependencies upon allowable Claim 1.

Claim Rejection Under 35 U.S.C. §103

Claims 5 and 6 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over the disclosure contained in Lou. This rejection is respectfully traversed because Claims 5 and 6 are patently distinguishable over the disclosure contained in that document.

As stated hereinabove, Claims 5 and 6 depend from allowable Claim 1. At least by virtue of their dependencies upon allowable Claim 1, Claims 5 and 6 are also allowable. The Examiner is, therefore, respectfully requested to withdraw the rejections of Claims 5 and 6.

Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

Osamu S. Nakagawa

Dated: May 27, 2003 By

Timothy B. Kang
Registration No.: 46,423

MANNAVA & KANG
2930 Langdon Gate Drive
Fairfax, VA 22031
(703) 560-8503
(703) 991-1162 (facsimile)

Version With Markings to Show Changes Made

Pursuant to 37 CFR § 1.121, the following is a copy of all amendments with deletions indicated by bracketing and additions indicated by underlining.

IN THE SPECIFICATION:

The specification has been amended as follows:

The paragraph beginning on page 8, line 21 and ending on page 9, line two, has been replaced with the following paragraph:

Returning to Fig. 2, in step 235, a second layer of metal 350 is deposited on top of the patterned interlevel dielectric layer [330] 335 (see Fig. 3E) to form the signal via 355 and the electrode vias 340-344, and an upper electrode 360 of a high-k constant MIM capacitor 370. The second layer of metal is finished by a second CMP process to complete the vias 338-344 and upper electrode 360, in step 240.

IN THE CLAIMS:

Claims 1-13 have been amended as follows:

1. (Amended) A method of forming a by-pass capacitor on a multi-level metallization device, said method comprising:

forming a first electrode in a first [metal] dielectric layer of said multi-level metallization device;

depositing a substantially thin [dielectric material] insulator layer over said first [metal] dielectric layer of said multi-level metallization device; and

forming a second electrode [on] in a second [metal] dielectric layer, wherein said second [metal] dielectric layer is formed over said substantially thin [dielectric material] insulator layer.

2. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, said method further comprising:

patterning said substantially thin [dielectric material] insulator layer to substantially cover said first electrode; and

adjusting a thickness of said substantially thin [dielectric material] insulator layer.

3. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 2, wherein a dielectric constant of said substantially thin [dielectric material] insulator layer is substantially high.

4. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 3, wherein said substantially thin [dielectric material] insulator layer includes silicon nitride.

5. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 3, wherein said thickness of said substantially thin [dielectric material] insulator layer is between 50 and 100 angstroms.

6. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 3, wherein said dielectric constant of said substantially thin [dielectric material] insulator layer is between 4 and 100.

7. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, said method further comprising:

depositing [an interlevel] the second dielectric [material] layer over said substantially thin [dielectric material] insulator layer; and

etching at least one via, said at least one via adapted to receive said second [metal layer] electrode.

8. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 7, said method further comprising:

[patterning said second metal layer to form said second electrode; and]

polishing said second [metal layer] electrode.

9. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, wherein said forming said first electrode comprises:

etching said first electrode in [a] the first dielectric layer of said multi-level metallization device.

10. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, [wherein said first electrode is formed in a parallel line configuration] further comprising:

forming the first electrode in a parallel line configuration.

11. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, [wherein said second electrode is formed in a parallel line configuration] further comprising:

forming the second electrode in a parallel line configuration.

12. (Amended) The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, wherein said substantially thin [dielectric material] insulator layer comprises a composite of materials.